

Mini Project

On

Sampling Circuit

(Sem : V, Third Year of Engineering)

By

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CERTIFICATE

This is to certify that the mini project entitled **Sampling Circuit** is a work of **Karan Shah (60002120095)** submitted to the EXTC department, D.J. Sanghvi C.O.E., during sixth semester of the academic year 2014-2015, **for the Third Year Of Engineering** course.

Abstract

The basic idea of this report is to understand the process of sampling. This report will have in understanding the concept of Quantization, Nyquist theorem, Sampling rate, Undersampling, Oversampling and the various types of distortion occurring in sampling.

In this report we have discussed about in brief the circuit being implemented and the specifications of certain components. It will also cover in brief the softwares being used as well the process of Etching and PCB design.

After implementing the circuit, we also discuss the ways to improve the output of the circuit as well as the advantages and disadvantages of the techniques for implementing the Sample and Hold Circuit.

Acknowledgements

Any task requires effort from many people and this is no different. First and foremost we feel immense pleasure and heartfelt gratitude towards our project guide Mr. Rahul S. Taware for his constant inspiration, guidance, constructive criticism and painstaking efforts to help us during this study and thank him for the same.

We would like to thank God for giving us physical and mental strength to get through the report. We would also like to thank H.O.D of Electronics and Telecommunication, Mr. Amit Deshmukh for allowing us to avail the facilities of the college for conducting our research. Last but not the least we would like to thank Mr. Tushar Sawant and Miss. Yukti Bandi for their constant support. We also acknowledge the contribution of our staff members, both teaching and non-teaching, and our friends who have directly or indirectly helped us in compiling of our report.

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1. Introduction

Sampling is the reduction of a continuous signal to a discrete signal. A common example is the conversion of a sound wave (a continuous signal) to a sequence of samples (a discrete-time signal). A sample refers to a value or set of values at a point in time and/or space. A sampler is a subsystem or operation that extracts samples from a continuous signal. A theoretical ideal sampler produces samples equivalent to the instantaneous value of the continuous signal at the desired points. Sampling can be done for functions varying in space, time, or any other dimension, and similar results are obtained in two or more dimensions.

This project aims to understand the basic process of sampling with the help of a simple circuit consisting of FET BFW 11, Op-Amp IC 741, resistors and capacitors. This report will also help in understanding how can we improve the same circuit using different components.

We hope you can gain some knowledge about sampling circuit as well as its practical application about the sampling process.

2. Theory

Sampling can be done for functions varying in space, time, or any other dimension, and similar results are obtained in two or more dimensions. For functions that vary with time, let $s(t)$ be a continuous function (or "signal") to be sampled, and let sampling be performed by measuring the value of the continuous function every T seconds, which is called the sampling interval. Then the sampled function is given by the sequence: $s(nT)$, for integer values of n .

2.1. Sampling Rate and Nyquist Theorem

The sampling frequency or sampling rate, f_s , is the average number of samples obtained in one second (samples per second), thus $f_s = 1/T$. Reconstructing a continuous function from samples is done by interpolation algorithms. The Whittaker–Shannon interpolation formula is mathematically equivalent to an ideal low pass filter whose input is a sequence of Dirac delta functions that are modulated (multiplied) by the sample values. When the time interval between adjacent samples is a constant (T), the sequence of delta functions is called a Dirac comb. Mathematically, the modulated Dirac comb is equivalent to the product of the comb function with $s(t)$. That purely mathematical abstraction is sometimes referred to as impulse sampling.

Most sampled signals are not simply stored and reconstructed. But the fidelity of a theoretical reconstruction is a customary measure of the effectiveness of sampling. That fidelity is reduced when $s(t)$ contains frequency components whose periodicity is smaller than 2 samples; or equivalently the ratio of cycles to samples exceeds $1/2$ (see Aliasing). The quantity $1/2$ cycles/sample $\times f_s$ samples/sec = $f_s/2$ cycles/sec (hertz) is known as the Nyquist frequency of the sampler. Therefore $s(t)$ is usually the output of a low pass filter, functionally known as an anti-aliasing filter. Without an anti-aliasing filter, frequencies higher than the Nyquist frequency will influence the samples in a way that is misinterpreted by the interpolation process.

If a function $x(t)$ contains no frequencies higher than B cps, it is completely determined by giving its ordinates at a series of points spaced $1/(2B)$ seconds apart.

A sufficient sample-rate is therefore $2B$ samples/second, or anything larger. Conversely, for a given sample rate f_s the band limit for perfect reconstruction is $B \leq f_s/2$. When the band limit is too high (or there is no band limit), the reconstruction exhibits imperfections known as aliasing. Modern statements of the theorem are sometimes careful to explicitly state

that $x(t)$ must contain no sinusoidal component at exactly frequency B , or that B must be strictly less than $\frac{1}{2}$ the sample rate. The two thresholds, $2B$ and $f_s/2$ are respectively called the Nyquist rate and Nyquist frequency. And respectively, they are attributes of $x(t)$ and of the sampling equipment. The condition described by these inequalities is called the Nyquist criterion, or sometimes the Raabe condition. The theorem is also applicable to functions of other domains, such as space, in the case of a digitized image. The only change, in the case of other domains, is the units of measure applied to t , f_s , and B .

The symbol $T = 1/f_s$ is customarily used to represent the interval between samples and is called the sample period or sampling interval. And the samples of function $x(t)$ are commonly denoted by $x[n] = x(nT)$ (alternatively " x_n " in older signal processing literature), for all integer values of n . The mathematically ideal way to interpolate the sequence involves the use of sinc functions, like those shown in Fig 2. Each sample in the sequence is replaced by a sinc function, centered on the time axis at the original location of the sample, nT , with the amplitude of the sinc function scaled to the sample value, $x[n]$. Subsequently, the sinc functions are summed into a continuous function. A mathematically equivalent method is to convolve one sinc function with a series of Dirac delta pulses, weighted by the sample values. Neither method is numerically practical. Instead, some type of approximation of the sinc functions, finite in length, is used. The imperfections attributable to the approximation are known as interpolation error.

Practical digital-to-analog converters produce neither scaled and delayed sinc functions, nor ideal Dirac pulses. Instead they produce a piecewise-constant sequence of scaled and delayed rectangular pulses (the zero-order hold), usually followed by an "anti-imaging filter" to clean up spurious high-frequency content.^[1]

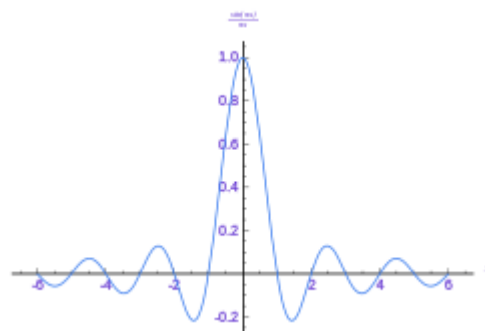


Figure 1: sinc function^[1]

In practice, the continuous signal is sampled using an analog-to-digital converter (ADC), a device with various physical limitations. This results in deviations from the theoretically perfect reconstruction, collectively referred to as distortion.

2.2. Types of Distortion

Various types of distortion can occur, including:

- Aliasing. Some amount of aliasing is inevitable because only theoretical, infinitely long, functions can have no frequency content above the Nyquist frequency. Aliasing can be made arbitrarily small by using a sufficiently large order of the anti-aliasing filter.
- Aperture error results from the fact that the sample is obtained as a time average within a sampling region, rather than just being equal to the signal value at the sampling instant. In a capacitor-based sample and hold circuit, aperture error is introduced because the capacitor cannot instantly change voltage thus requiring the sample to have non-zero width.
- Jitter or deviation from the precise sample timing intervals.
- Noise, including thermal sensor noise, analog circuit noise, etc.
- Slew rate limit error, caused by the inability of the ADC input value to change sufficiently rapidly.
- Quantization as a consequence of the finite precision of words that represent the converted values.
- Error due to other non-linear effects of the mapping of input voltage to converted output value (in addition to the effects of quantization).

Although the use of oversampling can completely eliminate aperture error and aliasing by shifting them out of the pass band, this technique cannot be practically used above a few GHz, and may be prohibitively expensive at much lower frequencies. Furthermore, while oversampling can reduce quantization error and non-linearity, it cannot eliminate these entirely. Consequently, practical ADCs at audio frequencies typically do not exhibit aliasing, aperture error, and are not limited by quantization error. Instead, analog noise dominates. At RF and microwave frequencies where oversampling is impractical and filters are expensive, aperture error, quantization error and aliasing can be significant limitations.

Jitter, noise, and quantization are often analyzed by modeling them as random errors added to the sample values. Integration and zero-order hold effects can be analyzed as a form of low-

pass filtering. The non-linearities of either ADC or DAC are analyzed by replacing the ideal linear function mapping with a proposed nonlinear function.^[1]

2.3. Oversampling and Undersampling

Oversampling is the process of sampling a signal with a sampling frequency significantly higher than the Nyquist rate. Theoretically a bandwidth-limited signal can be perfectly reconstructed if sampled above the Nyquist rate, which is twice the highest frequency in the signal. Oversampling improves resolution, reduces noise and helps avoid aliasing and phase distortion by relaxing anti-aliasing filter performance requirements.

In signal processing, undersampling or bandpass sampling is a technique where one samples a bandpass-filtered signal at a sample rate below its Nyquist rate (twice the upper cut-off frequency), but is still able to reconstruct the signal.

When one undersamples a bandpass signal, the samples are indistinguishable from the samples of a low-frequency alias of the high-frequency signal. Such sampling is also known as bandpass sampling, harmonic sampling, IF sampling, and direct IF-to-digital conversion.

2.4. Quantization

Quantization, in mathematics and digital signal processing, is the process of mapping a large set of input values to a (countable) smaller set – such as rounding values to some unit of precision. A device or algorithmic function that performs quantization is called a quantizer. The round-off error introduced by quantization is referred to as quantization error.

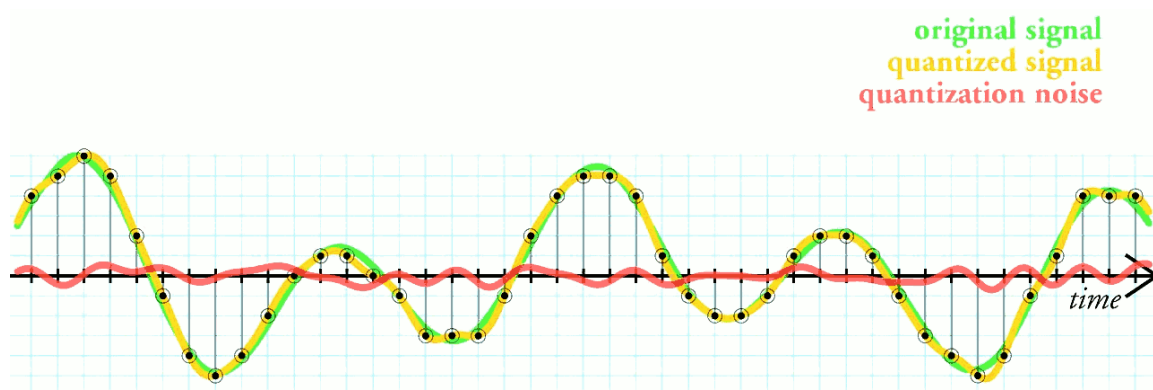


Figure 2: quantization input and output^[2]

In analog-to-digital conversion, the difference between the actual analog value and quantized digital value is called quantization error or quantization distortion. This error is either due

to rounding or truncation. The error signal is sometimes modeled as an additional random signal called quantization noise because of its stochastic behaviour. Quantization is involved to some degree in nearly all digital signal processing, as the process of representing a signal in digital form ordinarily involves rounding. Quantization also forms the core of essentially all lossy compression algorithms. Quantization is a many-to-few mapping, it is an inherently non-linear and irreversible process (i.e., because the same output value is shared by multiple input values, it is impossible in general to recover the exact input value when given only the output value).

The set of possible input values may be infinitely large, and may possibly be continuous and therefore uncountable (such as the set of all real numbers, or all real numbers within some limited range). The set of possible output values may be finite or countably infinite. The input and output sets involved in quantization can be defined in a rather general way. For example, vector quantization is the application of quantization to multi-dimensional (vector-valued) input data.

There are two substantially different classes of applications where quantization is used:

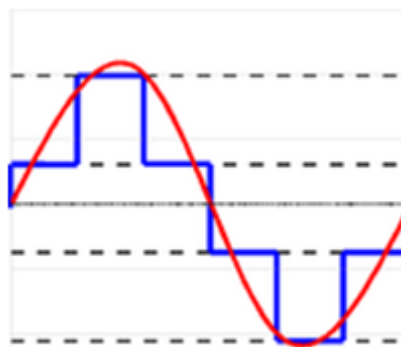


Figure 3: 2-bit resolution with four levels of quantization compared to analog^[2]

The first type, which may simply be called rounding quantization, is the one employed for many applications, to enable the use of a simple approximate representation for some quantity that is to be measured and used in other calculations. This category includes the simple rounding approximations used in everyday arithmetic. This category also includes analog-to-digital conversion of a signal for a digital signal processing system (e.g., using a sound card of a personal computer to capture an audio signal) and the calculations performed within most digital filtering processes. Here the purpose is primarily to retain as much signal fidelity as possible while eliminating unnecessary precision and keeping the dynamic range of the signal within practical limits (to avoid signal clipping or arithmetic overflow). In such uses,

substantial loss of signal fidelity is often unacceptable, and the design often centers around managing the approximation error to ensure that very little distortion is introduced.

The second type, which can be called rate–distortion optimized quantization, is encountered in source coding for "lossy" data compression algorithms, where the purpose is to manage distortion within the limits of the bit rate supported by a communication channel or storage medium. In this second setting, the amount of introduced distortion may be managed carefully by sophisticated techniques, and introducing some significant amount of distortion may be unavoidable.

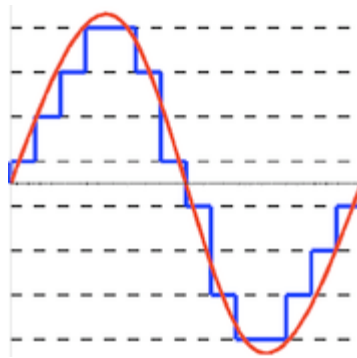


Figure 4: 3-bit resolution with eight levels^[1]

3. IMPLEMENTATION

A sample and hold circuit is a circuit which samples an input signal and holds onto its last sampled value until the input is sampled again. Sample and hold circuits are commonly used in analogue to digital converts, communication circuits, PWM circuits etc.

3.1. Sample and Hold Circuit

The circuit shown below is of a sample and hold circuit based on IC 741 Op-Amp , FET BFW 11 and few passive components.

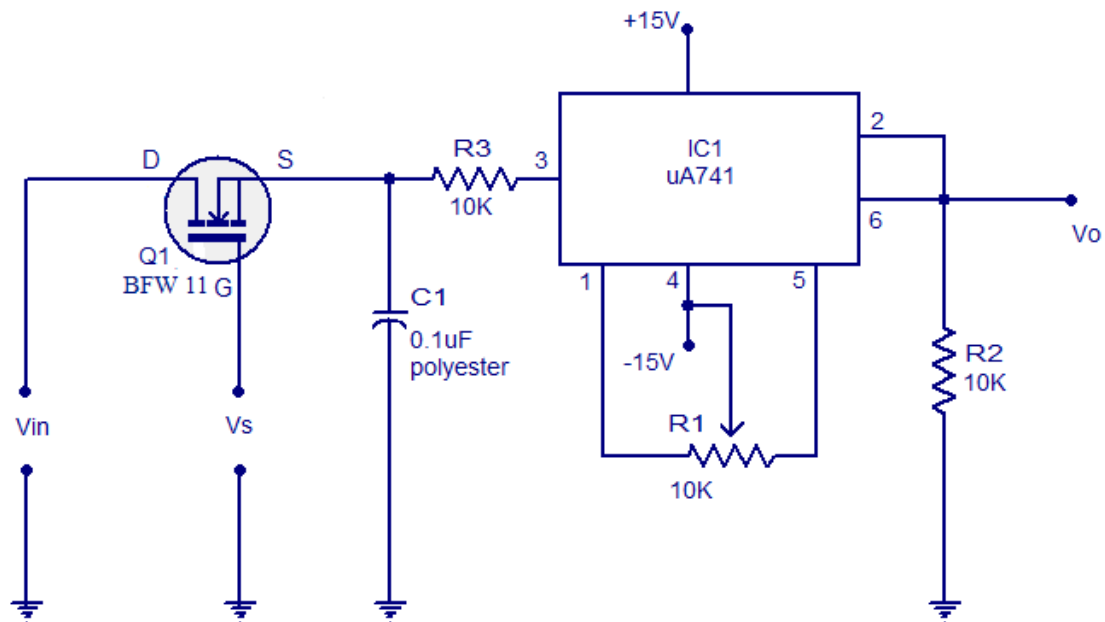


Figure 5: Sample and hold Circuit⁽²⁾

In the circuit FET BFW 11 ($Q1$) works as a switch while Op-Amp IC 741 is wired as a voltage follower. The signal to be sampled (V_{in}) is applied to the drain of FET while the sample and hold control voltage (V_s) is applied to the source of the FET. The source pin of the FET is connected to the non-inverting input of the Op-Amp through the resistor $R3$. $C1$ which is a polyester capacitor serves as the charge storing device. Resistor $R2$ serves as the load resistor while preset $R1$ is used for adjusting the offset voltage.

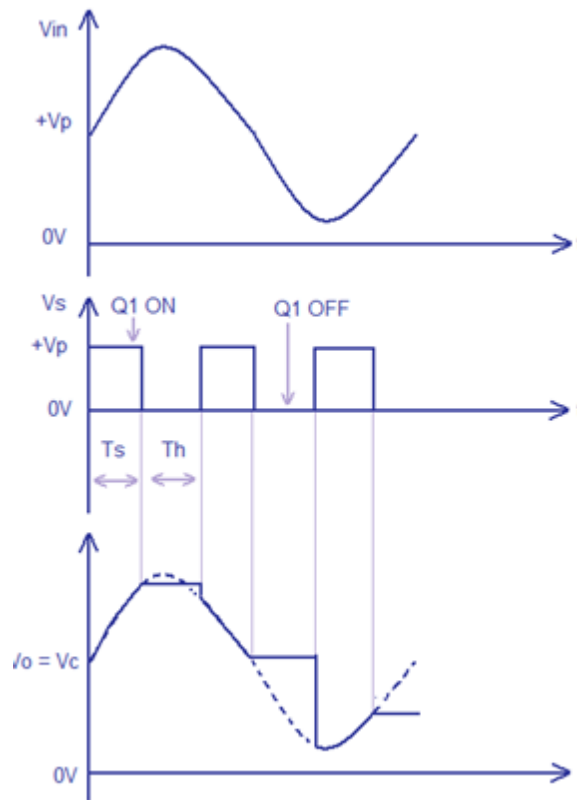


Figure 6: input and output wave form^[2]

During the positive half cycle of the V_s , the FET is ON which acts like a closed switch and the capacitor C_1 is charged by the V_{in} and the same voltage (V_{in}) appears at the output of the Op-Amp. When V_s is zero FET is switched off and the only discharge path for C_1 is through the inverting input of the Op-Amp. Since the input impedance of the Op-Amp is too high the voltage V_{in} is retained and it appears at the output of the Op-Amp. The time periods of the V_s during which the voltage across the capacitor (V_c) is equal to V_{in} are called sample periods (T_s) and the time periods of V_s during which the voltage across the capacitor C_1 (V_c) is held constant are called hold periods (T_h).^[2]

3.2. Implementation of circuit using Proteus.

After finding the circuit we implemented the circuit in Proteus 8. Proteus 8 is the best simulation software for various designs. After simulating the circuit in Proteus 8 Software we can directly convert the circuit to PCB design with it so it could be an all in one package for students and hobbyists. The image shown below is the circuit being implemented in Proteus software.

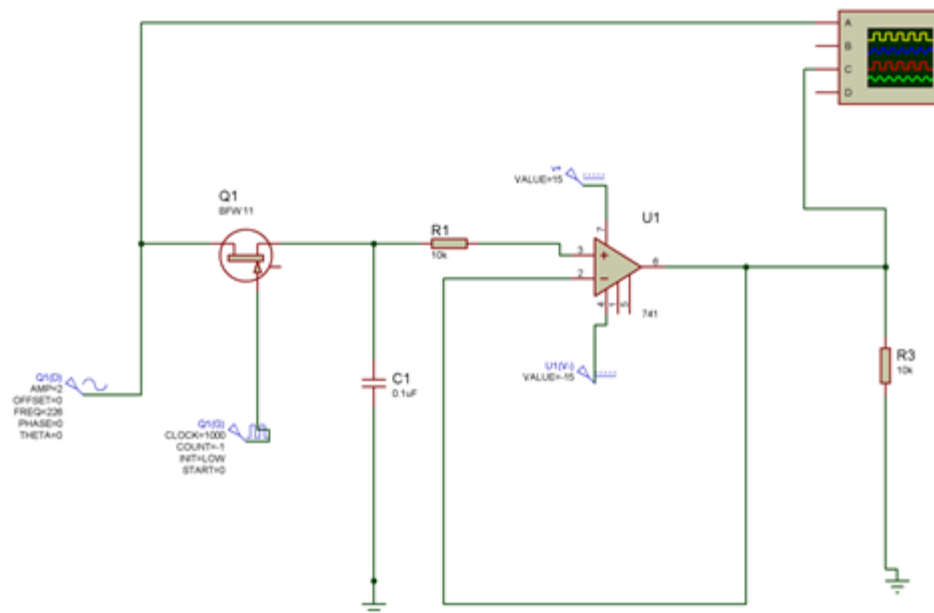


Figure 7: Proteus implemented Circuit diagram

The output obtained after simulating the above circuit is given below.

Yellow line is the input V_{in} and red line is the sampled output.

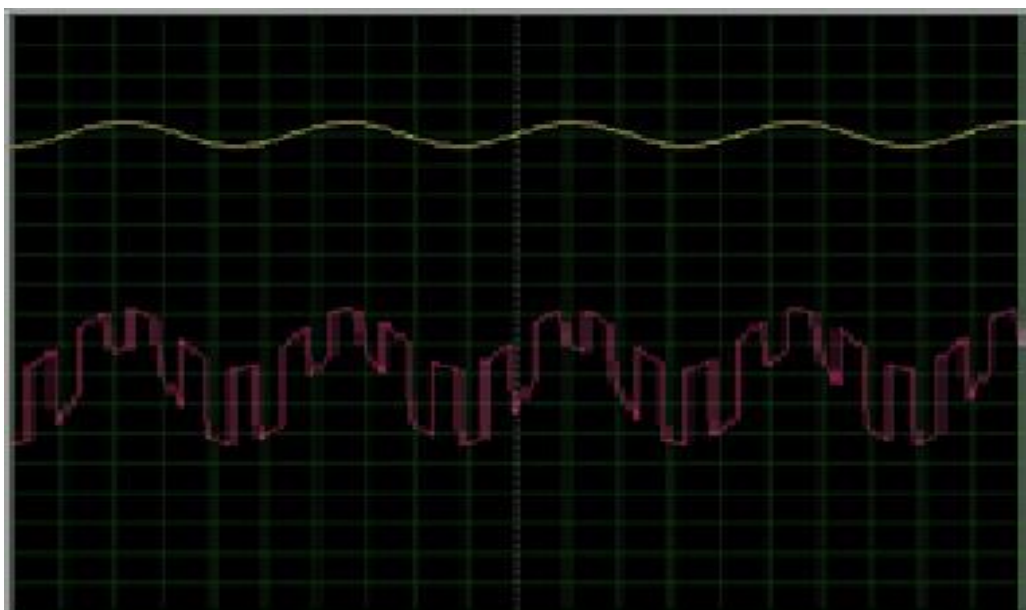


Figure 8: input and output waveform

3.3. Implementation of Circuit on Bread Board and Specifications of components.

After obtaining proper output we implemented the circuit on a breadboard. We used the components with the following specifications.

- FET BFW 11^[3]

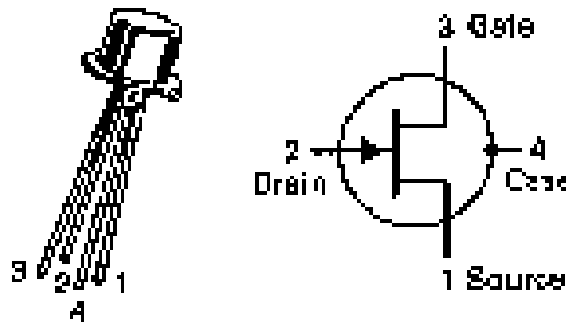


Figure 9: Structure & pin^[3]

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	30	V_{dc}
Drain-Gate Voltage	V_{DG}	30	V_{dc}
Reverse Gate-Source Voltage	V_{GSR}	-30	V_{dc}
Forward Gate Current	I_{GF}	10	mA_{dc}
Total device biaspoint @ 25 °C	P_D	300	mW
@ 26 °C		1.71	mW/ °C
Temperature Range	T_J	-0.5 to +150	°C

- **RESISTORS^[4]**

1. 10K Resistor

Resistance (ohms)	10K	Power (watts)	0.5W, 1/2W
Composition	Carbon Film	Temperature Coefficient	350ppm/°C
Tolerance	±5%	Size / Dimension	0.130" Dia x 0.354" L (3.30mm x 9.00mm)
Lead Style	Through Hole	Package / Case	Axial
Resistance In Ohms	10.0K	Case	Axial
Lead Free Status / RoHS Status	Lead free / RoHS Compliant	Features	-
Height	-	Other names	10K CR-1/2W-B 5% 10KH CFR-50JB 10K CFR-50JB-5210K

2. 1K Resistor

Resistance (ohms)	1K	Power (watts)	1W
Composition	Metal Film	Features	Flame Proof
Temperature Coefficient	±100ppm/°C	Tolerance	±5%
Size / Dimension	0.094" Dia x 0.248" L (2.40mm x 6.30mm)	Lead Style	Through Hole
Package / Case	Axial	Resistance In Ohms	1.00K
Case	Axial	Lead Free Status / RoHS Status	Lead free / RoHS Compliant
Height	-	Other names	1KWTR

- **Capacitor^[4]**

Operating Temperature -25°C to $+85^{\circ}\text{C}$

Capacitance Measured at $1 \pm 0.1 \text{ MHz}$, 1 V_{rms} at 25°C

Rated voltage 50V, 63V and 100V

Quality Factor Measured at $1 \pm 0.1 \text{ MHz}$, 1 V_{rms} at 25°C

$C < 30 \text{ pF}$ $Q = 400 + 20C$, $C > 30 \text{ pF}$ $Q = 1000 \text{ min.}$

(C = Capacitance)

Tested voltage :250% of rated voltage with 50mA charging current max.

Insulation resistance: 10,000 Mega ohms min. at rated voltage 60 sec.

Insulation coating: Phenolic coating applied by a wet dip method

- **IC 741^[5]**

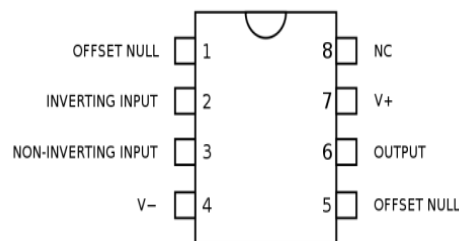


Figure 10: Pin config. Of IC 741

Supply Voltage: $\pm 22 \text{ V}$

Power Dissipation: 500 mW

Differential Input Voltage: $\pm 30 \text{ V}$

Input Voltage: $\pm 15 \text{ V}$

Output Short Circuit Duration: Continuous

Operating Temperature Range: -55°C to $+125^{\circ}\text{C}$

Storage Temperature Range: -65°C to $+150^{\circ}\text{C}$

Junction Temperature 150°C

The figure shown below is the circuit being tested on breadboard. We use the above mentioned components for testing the circuit.

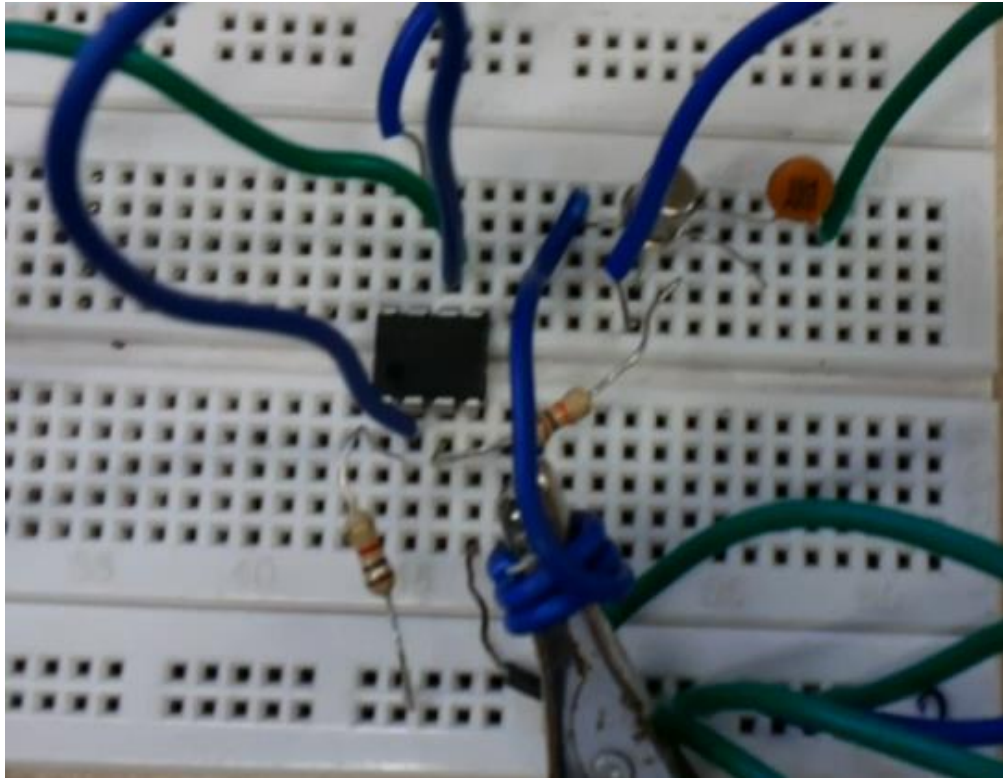


Figure 11: Bread board implemented circuit

By applying $V_{in} = 2\text{ V}$ at $f = 226\text{ Hz}$ and $V_s = 2\text{ V}$ at $f = 1\text{ KHz}$ we get the following output.

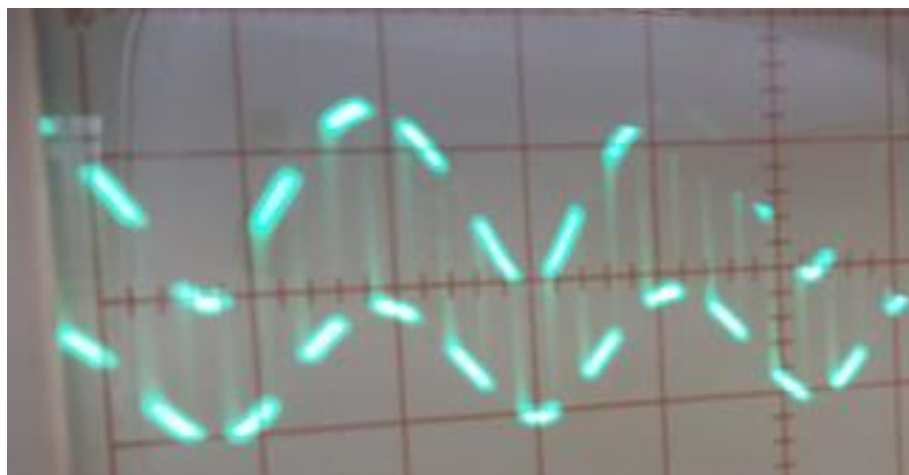


Figure 12: Output Waveform on CRO

3.4. Designing of PCB layout and Etching Process.

The next step in implementation was to design the PCB layout using Proteus Software. We designed the PCB Layout of the circuit as given below.

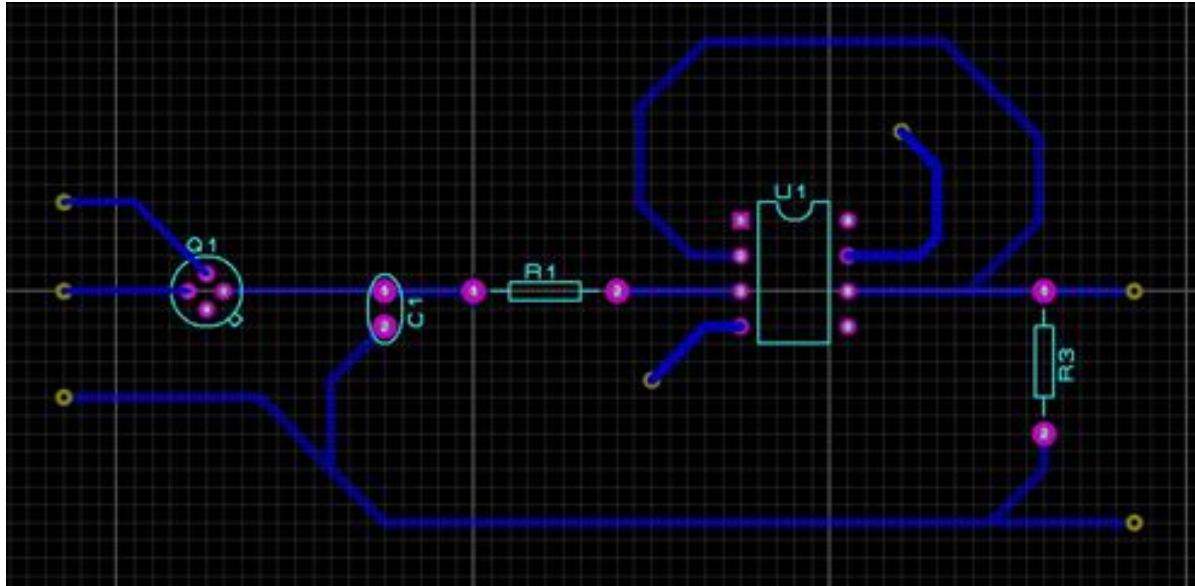


Figure 13: PCB LAYOUT

After taking the printout we ironed the PCB layout onto copper clad. After getting the layout on copper clad we started the process of Etching. Etching is the process of using strong acid or mordant to cut into the unprotected parts of a metal surface to create a design in intaglio in the metal (the original process—in modern manufacturing other chemicals may be used on other types of material). After removing from Etching process we check the connectivity and solder the components onto the PCB and check whether circuit is working or not. The figure below shows the soldering done on the track as well as the complete circuit.



Figure 14: Soldered Circuit

3.5. Checking of Final circuit on PCB.

We got a proper sampled sine wave after soldering the components onto the PCB. The output and the setup of the circuit is given below.

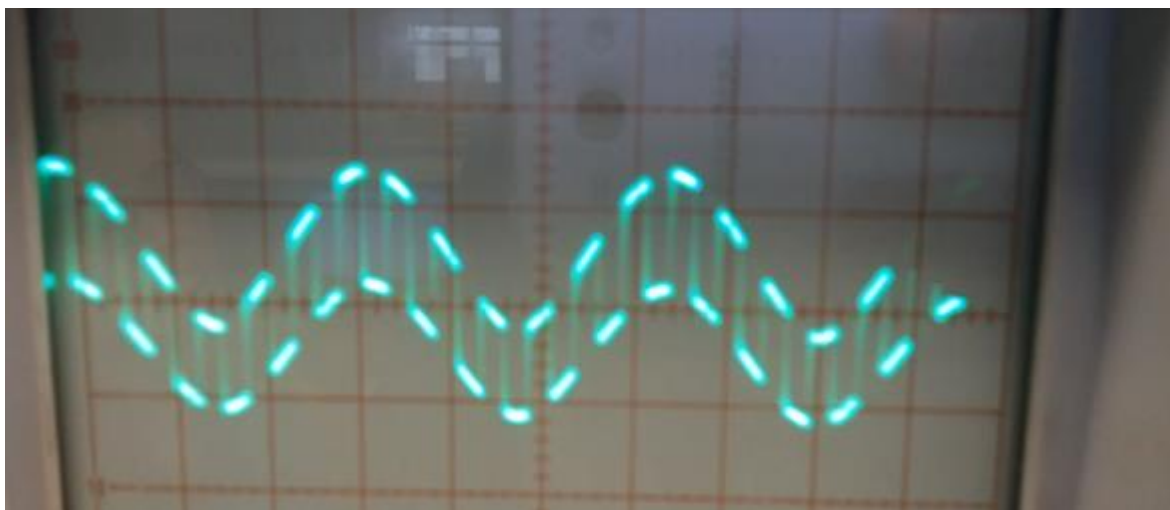


Figure 15: Final Output Waveform

The connections of the circuit are given below in the photo.



Figure 16: Setup of Sampling Circuit

Thus we have successfully implemented sampling circuit in software and hardware also.

4. Applications

1. Audio sampling

Digital audio uses pulse-code modulation and digital signals for sound reproduction. This includes analog-to-digital conversion (ADC), digital-to-analog conversion (DAC), storage, and transmission. In effect, the system commonly referred to as digital is in fact a discrete-time, discrete-level analog of a previous electrical analog. While modern systems can be quite subtle in their methods, the primary usefulness of a digital system is the ability to store, retrieve and transmit signals without any loss of quality.^[7]

2. Bit depth

Audio is typically recorded at 8-, 16-, and 20-bit depth, which yield a theoretical maximum Signal-to-quantization-noise ratio (SQNR) for a pure sine wave of, approximately, 49.93 dB, 98.09 dB and 122.17 dB.^[16] CD quality audio uses 16-bit samples. Thermal noise limits the true number of bits that can be used in quantization. Few analog systems have signal to noise ratios (SNR) exceeding 120 dB. However, digital signal processing operations can have very high dynamic range, consequently it is common to perform mixing and mastering operations at 32-bit precision and then convert to 16 or 24 bit for distribution.^[7]

3. Speech sampling

Speech signals, i.e., signals intended to carry only human speech, can usually be sampled at a much lower rate. For most phonemes, almost all of the energy is contained in the 5Hz-4 kHz range, allowing a sampling rate of 8 kHz. This is the sampling rate used by nearly all telephony systems, which use the G.711 sampling and quantization specifications.^[7]

4. Video sampling

Standard-definition television (SDTV) uses either 720 by 480 pixels (US NTSC 525-line) or 704 by 576 pixels (UK PAL 625-line) for the visible picture area. High-definition television (HDTV) uses 720p (progressive), 1080i (interlaced), and 1080p (progressive, also known as Full-HD). In digital video, the temporal sampling rate is defined the frame rate – or rather the field rate – rather than the notional pixel clock. The image sampling frequency is the repetition rate of the sensor integration period.^[7]

5. Conclusion

Thus in this report we come to know the different aspects of sampling as well its basic technique using Op-Amp. There are many places where the circuit can be improved in terms of cost as well as the performance.

One of the techniques the output can be perfected is by using MOSFET 2N4416A, it increases the accuracy of the output and we can get a proper sampled output. The other way to reduce sampling distortion is by increasing the amplitude of the clock signal. Other ways to improve the stability of the circuit is by integrating the Sample and Hold circuit, by using Switch capacitance or Miller capacitance. We can also add a feedback network to the circuit to get proper amplitude of the output. We can use a double buffered sample and hold circuit with CMOS switch.^[6] By using the above techniques we get the following output.

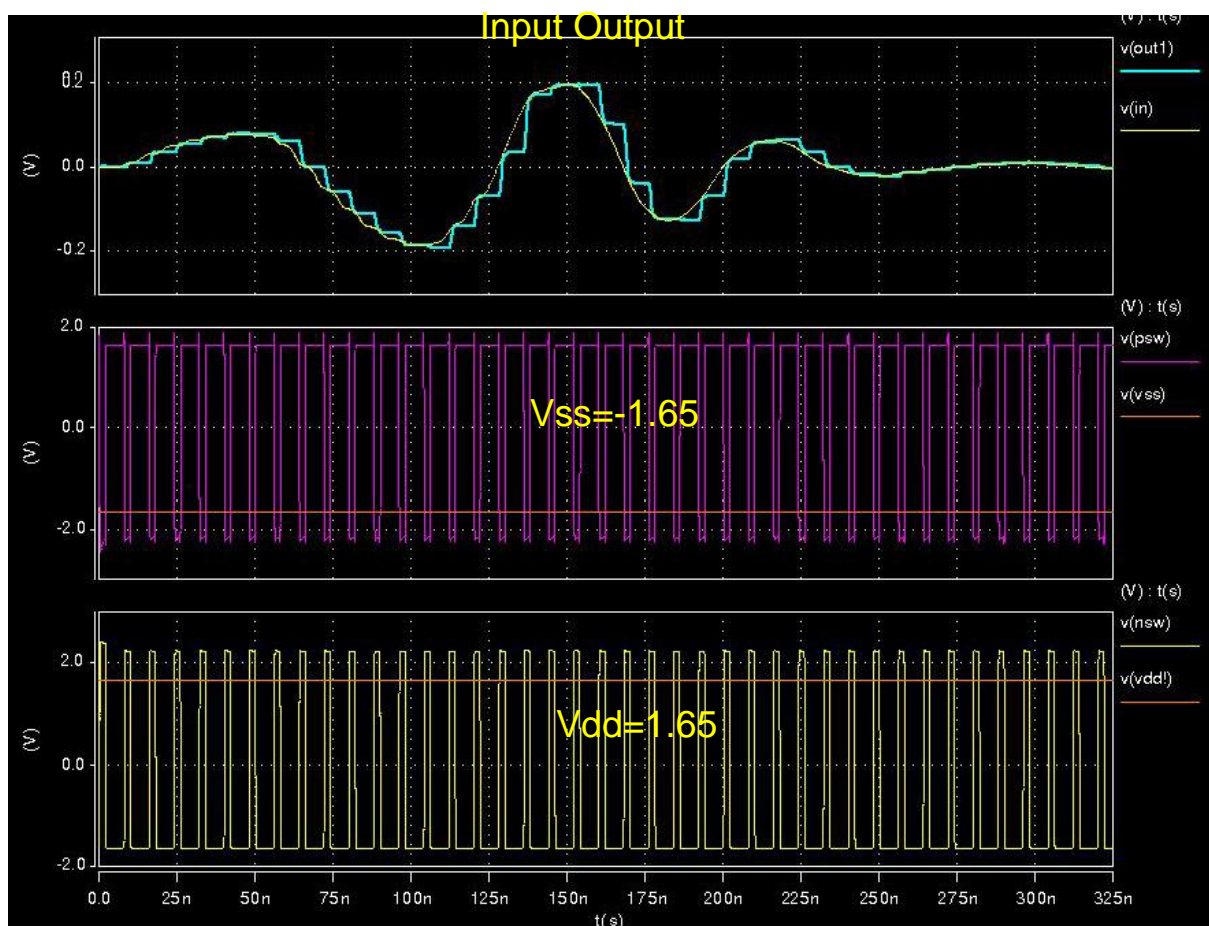


Figure 17: Improved Output via different Component^[6]

But there are many drawbacks by changing the technique as each method have different disadvantages as well which can increase the cost of the circuit. Some of the disadvantages are special Care must be taken to obtain stability of SHA. It needs a special circuitry to stabilize the input amplifier during the holding mode.

Sampling circuit can be studied and implemented using different active and passive components.

References

- [1] en.wikipedia.org
- [2] www.circuitstoday.com
- [3] html.alldatasheet.com
- [4] www.elcodis.com
- [5] www.datasheetarchive.com
- [6] www.cse.psu.edu
- [7] Linear integrated circuits by Ramakant Gaikawad