2:1 Switched Capacitor DC – DC Voltage Converter

Karan Shah
Northwestern University
karan.shah@u.northwestern.edu

Motivation

Recent advances in mobile electronics show explosive growth in the demand for compute power, data storage and, the number of RF and analog interfaces mandated by increasingly context-aware and perceptual user experience. These factors combined with the compact form factor demands and extreme sensitivity to cost and energy are driving innovations in mixed-signal SoCs at an unprecedented rate.

Also, conventional inductor based switched converters suffer from scalability limitations in size and power. Thus recently, switched capacitor DC-DC converters have emerged with increased current carrying capability.

Introduction

The basic idea regarding how to design Switched Capacitor DC-DC Voltage Converter is to obtain an output in the multiples you want based on the switching pattern of the switches and the configuration of the circuit.

There are various topologies like 2:1,3:2,5:4, etc. and vice-versa are shown in Figure 1.

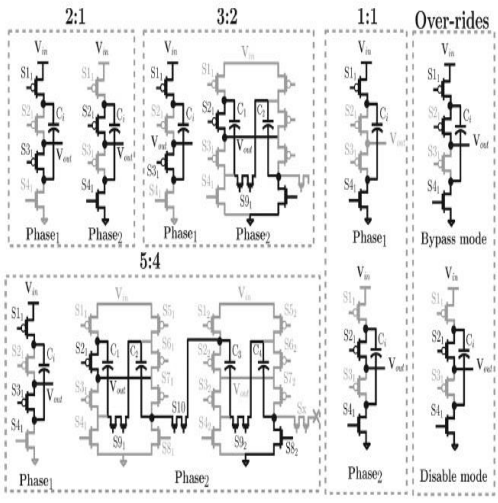

Fig. 5. Multiple transformation ratios.

Figure 1: Various Topologies

Challenges

Fully integrated circuits in paper reviews thus it was difficult to implement all of it in such short time. Deciding as to which circuit to implement because every paper went for different approaches.

Issues with using Virtuoso, as it was the first time using virtuoso and with pdf tutorial one cannot get a total overview. And it was a huge learning curve. As of now, I can for sure design circuits using virtuoso. Pressure of completing project in virtually 2 months was immense as at first it was difficult to approach.

Review of existing work

I went through these papers and tried to extract the main circuits and had discussion with professor as to which circuit to go for. After long chat, finalized the below circuit. The comparison for different circuit are shown in Table 1.

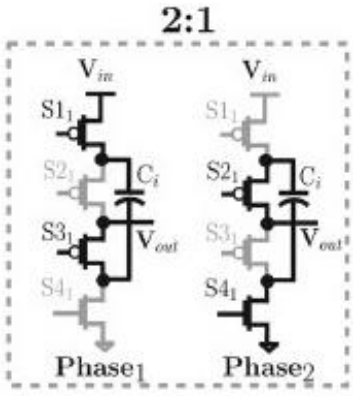

Figure 1: Various Topologies

Analysis

I went through many circuits and went through many papers before finalizing the approach. I reviewed the results for LDO, Fully integrated VR, for single as well as multi cores. Goal at first was to design a circuit which can incorporate all the topologies, and which can switch based on the output requirement. With the current circuit we get ideal output at a load of around

1-1.1kΩ. Tried varying width of transistors, along with that varied values of capacitors and load. Also, V_{ph1} and V_{ph2} should be out of phase with each other.

The combination of Width of PMOS= 11µm and NMOS= 10µm, value of flying capacitor=1 nF and that of output capacitor = 4nF gives output of 0.574 V.

Design Model

The model designed is a 2:1 DC-DC voltage converter.

Input voltage is provided with 1.2V and 3 PMOS and 1 NMOS transistors makes for a total of four switches which are provided with V_{pulse} (V_{phase}) thus making circuit work in 2 phases. During the first phase Transistors 1 and 3 works thus, charging the capacitor while in second phase transistors 2 and 4 operates thus giving the output and the ideal output of 0.6 V is obtained near load of 1-1.1kΩ. Also, there are two capacitors used in total; one acts as a flying capacitor while other as an output capacitor.

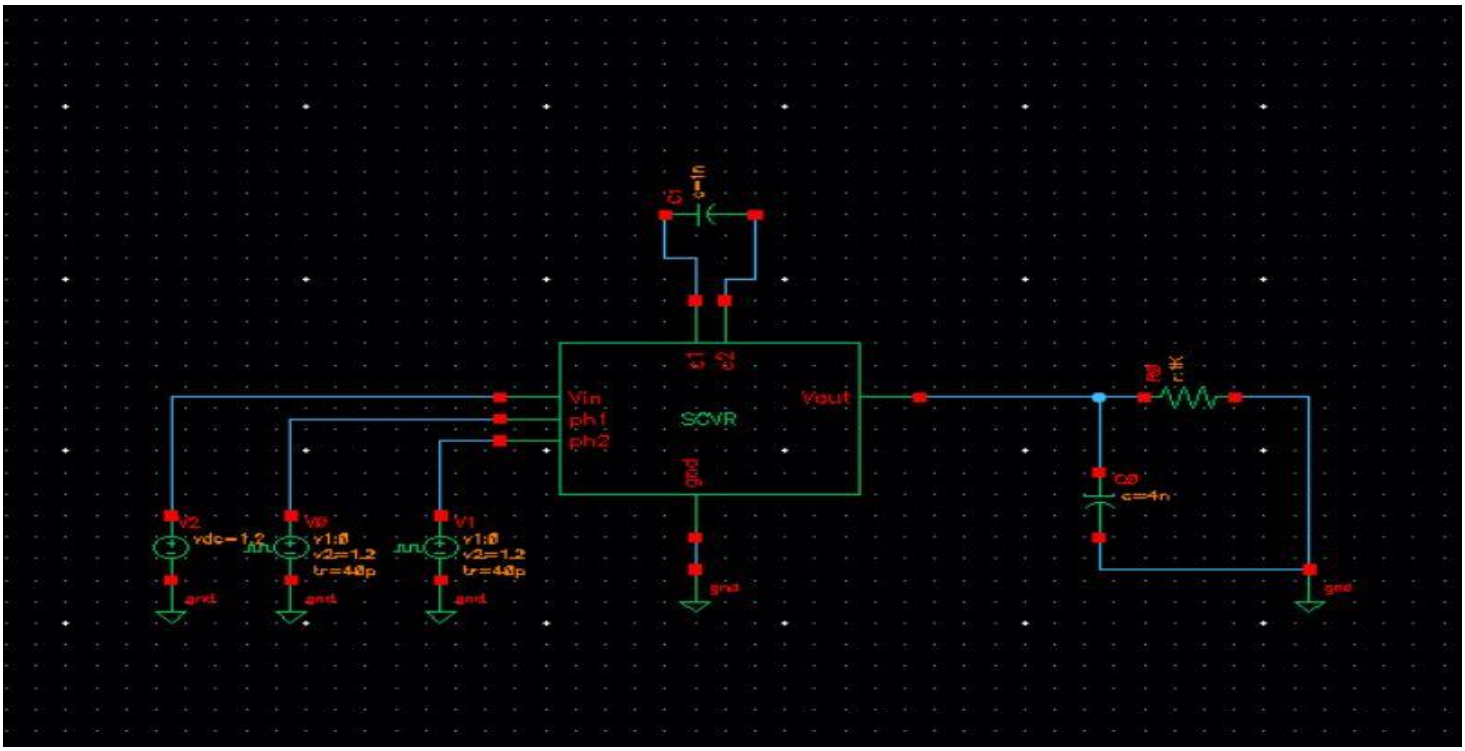

Figure 3: Circuit Diagram

COMPARISON WITH OTHER FULLY INTEGRATED SWITCHED CAPACITOR VOLTAGE REGULATORS

Reference	L. Chang VLSI 2010	Y. Ramadass ISSCC 2010	D. Somasekhar VLSI 2009	H. -P. Le ISSCC 2010	This work
Process	45nm SOI	45nm	32nm	32nm SOI	22nm trigate
Passives type	Deep trench	Gate Oxide SOI	Metal Finger	Gate Oxide	MIM
Maximum frequency	100MHz	30MHz	1GHz	225MHz	250MHz
Input Voltage	2V	1.8V	1-1.2V	2V	1.23V
Output	0.95V/2.7mA	0.8-1V/8mA	1.5V/5mA	0.4-1.1V/0.28A	0.45-1V, 88mA
Power Efficiency %	90	69	60	81	70@0.55V,84@1.1V
Response time	Unregulated	120-200ns	Unregulated	Unregulated	3-5ns†
Droop	-	250mV	-	-	≪25mV†
Current densityA/mm^2	2.3	0.050	1.12	0.73	0.88
Area Overhead	13%	6x	26%	41%	3.6%

†

Table 1: Comparison

Results and Layout

This section shows the layout of the regulator along with the output waveform. Figure 4 shows the transient response. Figure 5 shows the transient response along with DC output. Figure 6 shows the regulator design used in the circuit implemented. Figure 7 shows the layout of the circuit.

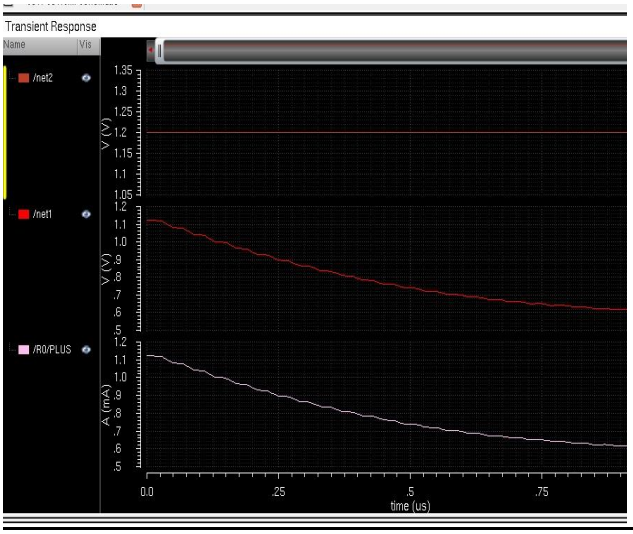

Figure 4: Transient Response

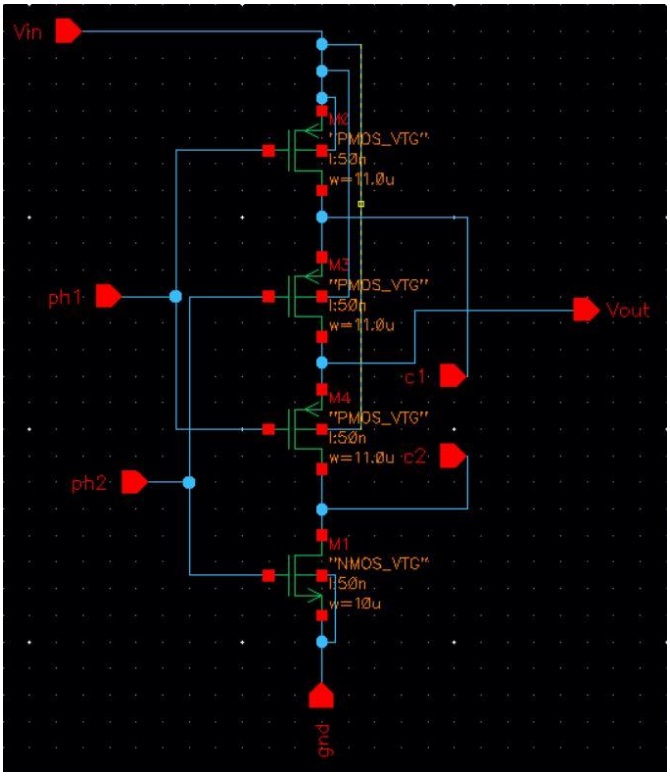

Figure 6: Regulator Design

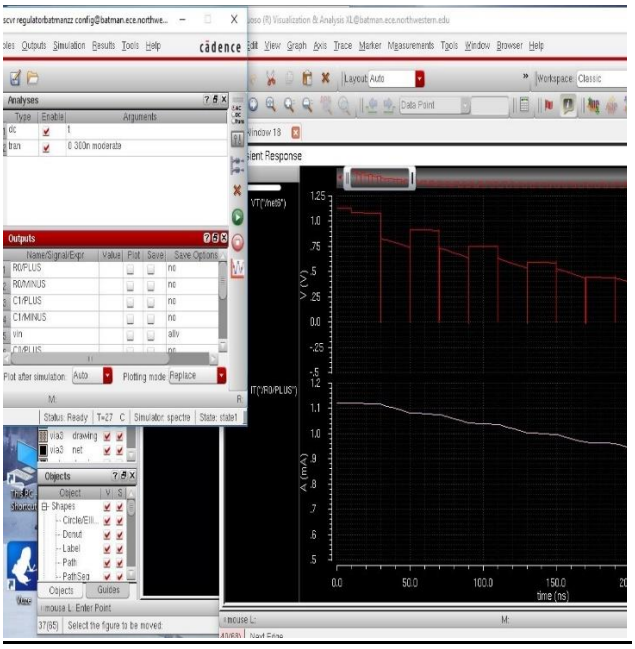

Figure 5: Output Waveform

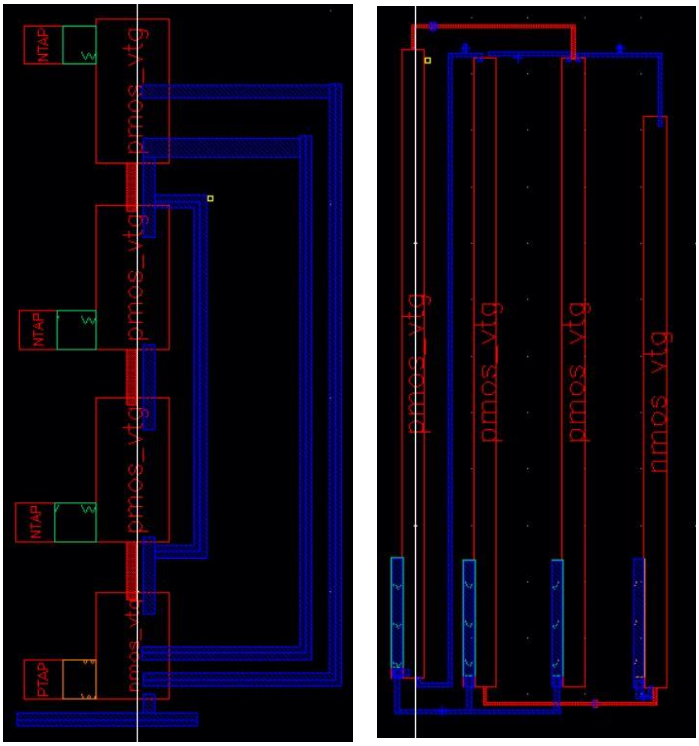

Figure 7: Layout

Conclusion

The simulation result of the output is about 0.47V. Using the similar technique, we can design converters for other configurations as well. Varying the values of capacitors, transistors, load, and V_{pulse} we can optimize the output. Feedback is the main part of a regulator. But couldn't incorporate because of the time constraint. We can tune the resistor and capacitor to obtain a better output value.

Acknowledgment

I would like to thank Prof. Jie Gu for his constant support and motivation. I would also like to thank thw EECS 495 class, EECS department and Northwestern University for their encouragement and support.

References

1. (Base for Project): Fully-Integrated Distributed Switched Capacitor DC-DC Converter with High Density MIM Capacitor in 22 nm Tri-Gate CMOS. IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 49, NO. 4, APRIL 2014
2. Fully Integrated Reconfigurable Switched-Capacitor DC-DC Converter Delivering 0.55W/mm2 at 81% Efficiency. ISSCC 2010 / February 9, 2010
3. A Sub-ns Response Fully Integrated Battery-Connected Switched-Capacitor Voltage Regulator Delivering 0.19W/mm2 at 73% Efficiency. ISSCC 2013 / February 20, 2013
4. 3.7μW 0.8V VCO-Integrator-Based High-Efficiency Capacitor-Free Low-Dropout Voltage Regulator.
5. On-Chip Hybrid Regulator Topology for Portable SoCs with Near-Threshold Operation.
6. System-Level Power Analysis of a Multicore Multipower Domain Processor with On-Chip Voltage Regulator.